In the Specification:

Please replace the paragraph at page 6, lines 3-14 with the following amended paragraph:

Referring now to Figures 1A through 1G, cross-sectional views illustrating processing steps in the fabrication of integrated circuit devices according to some embodiments of the present invention will be discussed. As illustrated in Figure 1A, a substrate [[100]] 10 having a fuse region is formed. The substrate may have a lower part structure that includes a transistor and a bit line. In embodiments of the present invention illustrated in Figure 1A, the bit line extends into the fuse region and is patterned. As further illustrated, the bit line includes a buffer pattern 12a and a line pattern 12b. The buffer pattern 12a and the line pattern 12b may include, for example, polysilicon, ruthenium (Ru), platinum (Pt), iridium (Ir), titanium nitride (TiN), tantalum nitride (TaN), tungsten nitride (WN) and the like. An insulation layer 14 may be formed or deposited on the buffer pattern 12a, the line pattern 12b and the substrate [[100]] 10. The insulation layer 14 may be, for example, an interlayer dielectric layer such as an oxide layer.